CLAIM(S):

1. An integrated circuit wafer comprising:
an integrated circuit die having a fuse circuit;
a first pad positioned in a scribe lane adjacent the integrated circuit die; and
a first conductor extending from the fuse circuit to the first pad.

2. The integrated circuit wafer of claim 1 and further comprising:
a second pad positioned in the scribe lane; and
a second conductor extending from the fuse circuit to the second pad.

3. The integrated circuit wafer of claim 2 wherein the first and second pads are a fuse pad and a supply pad, respectively.

4. The integrated circuit of claim 1 wherein the fuse circuit includes a fuse and circuitry for sensing whether the fuse is blown.

5. The integrated circuit of claim 3 wherein the fuse and the circuitry are aligned generally parallel to an edge of an integrated circuit die.

6. The integrated circuit of claim 5 wherein the conductor is oriented generally perpendicular to the edge.

7. An integrated circuit wafer comprising:
a plurality of integrated circuit dice separated from one another by scribe lanes, the dice having device trimming fuse circuits adjacent the scribe lanes; and

a plurality of pads positioned in the scribe lane and connected to the device trimming fuse circuits by conductors, so that following singularization of the dice from the wafer, the pads are disconnected from the device trimming fuse circuits.

8. The integrated circuit wafer of claim 7 wherein the plurality of pads include a fuse pad and a power supply pad connected to each fuse circuit.

9. The integrated circuit wafer of claim 8 wherein each fuse circuit includes a fuse connected to the fuse pad and the power supply pad by the conductors which cross the die edges.

10. The integrated circuit wafer of claim 9 wherein each fuse circuit includes circuitry for sensing whether the fuse is blown.

11. The integrated circuit wafer of claim 7 wherein the fuse circuits are aligned in rows generally parallel to the scribe lanes.

12. A trimmable integrated circuit comprising:

a plurality of fuses positioned adjacent a die edge of the integrated circuit;

a plurality of pads positioned in a scribe lane adjacent to the die edge; and

a plurality of conductors extending across the die edge for connecting the pads and the fuses to allow trimming of the integrated circuit by selective blowing of the fuses, the

conductors being severable during singularization of the integrated circuit.

13. The trimmable integrated circuit of claim 13 wherein the fuses are aligned in a row generally parallel to the die edge.

14. The trimmable integrated circuit of claim 12 wherein a pair of adjacent fuses share one common pad.

15. A method of manufacturing an integrated circuit, the method comprising:

forming on a wafer an integrated circuit having a fuse circuit adjacent a scribe lane and a pair of pads connected to the fuse circuit and located in the scribe lane;

testing the integrated circuit;

selectively supplying current through the pads to the fuse circuit, based upon the testing, to blow a fuse in the fuse circuit; and

severing the integrated circuit from the wafer within the scribe lane.

16. An integrated circuit manufactured by the method of claim 15.

17. A method of manufacturing integrated circuits, the method comprising:

forming a wafer having integrated circuits with a plurality of fuses and a plurality of pads connected to the fuses;

performing functional measurements of the integrated circuits;

trimming the integrated circuits based upon the functional measurements by selectively energizing the pads to blow selected fuses; and

severing the integrated circuits from the pads.

18. The method of claim 17, wherein the pads are positioned in scribe lanes adjacent the integrated circuits.

19. The method of claim 17, wherein the fuses are positioned adjacent the scribe lanes.

20. The method of claim 17, wherein the pads and the fuses are connected by conductors which extend from the integrated circuits into the scribe lanes.

21. An integrated circuit manufactured by the method of claim 17.

22. An integrated circuit die having a plurality of device trimming fuse circuits adjacent a die edge and conductors extending from the fuse circuits to the die edge, the conductors providing connection between the fuse circuits and pads which are severed from the die subsequent to selective blowing of fuses of the fuse circuits.